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Attorney Docket No. 0939H-071110US

Client Ref No. P99H4027/US/JJ

"Express Mail" Label No. EL624001188US

Date of Deposit: October 18, 2000

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

By: Sherry Barton

ASSISTANT COMMISSIONER FOR PATENTS
BOX PATENT APPLICATION
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is the
[ ] patent application of
[X] continuation patent application of
[ ] divisional patent application of
[ ] continuation-in-part patent application of

Inventor(s)/Applicant Identifier: In Sool Chung and Seong Dong Kim

For: IMAGE SENSOR WITH IMPROVED DYNAMIC RANGE BY APPLYING NEGATIVE VOLTAGE TO UNIT PIXEL

[X] This application claims priority from each of the following Application Nos./filing dates:
09/343,096, filed June 29, 1999
the disclosure(s) of which is (are) incorporated by reference.

[ ] Please amend this application by adding the following before the first sentence: "This application is a [ ] continuation [ ] continuation-in-part of and claims the benefit of U.S. Provisional Application No. 60/_____, filed _____, the disclosure of which is incorporated by reference."

Enclosed are:
6 page(s) of specification
3 page(s) of claims
1 page of Abstract
8 sheet(s) of [X] formal [ ] informal drawing(s).
An assignment of the invention to _____
A [ ] signed [X] unsigned Declaration & Power of Attorney
A [ ] signed [ ] unsigned Declaration.
A Power of Attorney.
A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [ ] is enclosed [ ] was filed in the prior application and small entity status is still proper and desired.
A certified copy of a _____ application.
Information Disclosure Statement under 37 CFR 1.97.
A petition to extend time to respond in the parent application.
Notification of change of [ ] power of attorney [ ] correspondence address filed in prior application.
Preliminary Amendment

In view of the Unsigned Declaration as filed with this application and pursuant to 37 CFR §1.53(f), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

DO NOT CHARGE THE FILING FEE AT THIS TIME.

William E. Winters
Reg No.: 42,232
Attorneys for Applicant

Telephone:
(415) 576-0200

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(415) 576-0300

SF 1149030 v1

Amendment

TOWNSEND and TOWNSEND and CREW LLP
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San Francisco, California 94111-3834
(415) 576-0200

Attorney Docket No. 0939H-071110US
Client Ref No. P99H4027/US/JJ

In re application of: In Sool Chung

Seong Dong Kim

Application No.:

Filed: 10 / 18 / 00

Group Art Unit:

Date: October 18, 2000

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Assistant Commissioner for Patents
Washington, D.C. 20231

Signed: Sherry Barton

For: IMAGE SENSOR WITH IMPROVED DYNAMIC RANGE BY APPLYING NEGATIVE VOLTAGE TO UNIT PIXEL

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith is a Preliminary Amendment in the above-identified application.

[ ] Enclosed is a petition to extend time to respond.
[ ] Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified statement previously submitted.
[ ] A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.

If any extension of time is needed, then this response should be considered a petition therefor.
The filing fee has been calculated as shown below:

(Col. 1)		(Col. 2)		(Col. 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA
TOTAL	* 7	MINUS	** 15	= 0
INDEP.	* 3	MINUS	*** 4	= 0
[ ] FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY			OTHER THAN SMALL ENTITY	
RATE	ADDIT. FEE	OR	RATE	ADDIT. FEE
x $9.00 =			x $18.00 =	$0.00
x $40.00 =			x $80.00 =	$0.00
+ $135.00 =			+ $270.00 =	
TOTAL ADDIT. FEE		OR	TOTAL	$0.00

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, then write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.

[X] No fee is due.

Please charge Deposit Account No. 20-1430 as follows:

[ ] Claims fee $ 0
[X] Any additional fees associated with this paper or during the pendency of this application.

NO extra copies of this sheet are enclosed.

TOWNSEND and TOWNSEND and CREW LLP

William E. Winters, Reg. No. 42,232
Attorneys for Applicant

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Assistant Commissioner for Patents
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On October 18, 2000

TOWNSEND and TOWNSEND and CREW LLP

By: Sherry Barton

PATENT
Attorney Docket No.: 0939H-071110US
Client Reference No.: P99H4027/US/JJ

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner:
Chung, In Sool et al.	Art Unit:
Filed: October 18, 2000	PRELIMINARY AMENDMENT
For: IMAGE SENSOR WITH IMPROVED DYNAMIC RANGE BY APPLYING NEGATIVE VOLTAGE TO UNIT PIXEL	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-referenced application, please enter the following amendments and remarks.

IN THE CLAIMS:

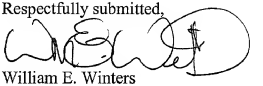
Cancel claims 7 through 14.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-273-7589 .

Respectfully submitted,



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SF 1148258 v1

Attorney Docket No.: 0939H-071110US
Client Reference No.: P99H4027/US/JJ

PATENT APPLICATION

Image Sensor With Improved Dynamic Range by Applying Negative Voltage to Unit Pixel

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Image Sensor With Improved Dynamic Range by Applying Negative Voltage to Unit Pixel

FIELD OF THE INVENTION

The present invention relates to an image sensor; and, more particularly, to a CMOS (Complementary Metal Oxide Semiconductor) image sensor with improved dynamic range by applying a negative voltage to a unit pixel.

DESCRIPTION OF THE PRIOR ART

Generally, a CMOS image sensor is an apparatus that converts an optical image into electrical signals using MOS (Metal Oxide Semiconductor) transistors. A CCD (Charge Coupled Device) image sensor, as a kind of image sensor, is widely known. As compared with the CCD image sensor, the CMOS image sensor may be easily driven with various scanning schemes and integrated with a signal processing circuit on one-chip. Therefore, the CMOS image sensor may be miniaturize in size and, consequently, a reduction in the fabricating cost and the power consumption may be realized using a compatible CMOS technology.

Referring to Fig. 1, a conventional unit pixel of a CMOS image sensor is composed of a pinned photodiode (PPD) and four NMOS transistors. The four NMOS transistors include a transfer transistor 102 for transferring photoelectric charges generated in the pinned photodiode to a sensing node, a reset transistor 104 for resetting the sensing node in order to sense a next signal, a drive transistor 106 that functions as a source follower and a select transistor 108 outputting data to an output terminal in response to an address signal.

The reset transistor 104 and the transfer transistor 102 are made up of a native NMOS transistor so that charge transfer efficiency is improved. The native NMOS transistor has about a zero threshold voltage, which helps prevent electron losses from being generated that would otherwise occur for transistors having a positive threshold voltage. A load transistor 110, which is positioned between an output terminal (OUT) of the unit pixel and the ground voltage level, receives a biasing signal from an external device and is used to bias the unit pixel. A capacitance of a floating diffusion is referred to as "C_{fd}".

Referring to Fig. 2, the conventional unit pixel of the CMOS image sensor includes a P^+ silicon substrate 201, a P-epi (epitaxial) layer 202, a P-well region 203, field oxide layers 204, a gate oxide layer 205, gate electrodes 206, an N^- diffusion region 207, a P^0

diffusion region 208, an N^+ diffusion region 209 and oxide layer spacers 210. A pinned photodiode (PPD) has a PNP junction structure in which the P-epi 202, the N^- diffusion region 207 and the P^0 diffusion region 208 are stacked. The P-epi layer 202, to which the ground voltage level is applied, is formed on the P^+ silicon substrate 201. Since a voltage of the P^+ silicon substrate 201 is fixed to the ground voltage level and a voltage variation range of the floating diffusion is limited, a voltage variation range of the output terminal of the unit pixel is very small. So, there is a problem that dynamic range of the unit pixel is also limited.

Since a power supply V_{DD} of the unit pixel is 2.5V, 3V or 5V in a sub-micron CMOS technology and a voltage of the pinned photodiode is fixed to the ground voltage level, a pinning voltage, which fully depletes the N^- diffusion region 207 of the pinned photodiode, should be at 0V or between a punch-through voltage of the transfer transistor 102 and the power supply V_{DD}. When the pinning voltage is very high, it is difficult for the photoelectric charges to be fully transferred to the floating sensing node in the power supply of 3.3V. That is, when the charge transfer efficiency becomes very low, a charge capacity becomes very small and the quantum efficiency is depreciated.

As a result, since the charge transfer efficiency and the quantum efficiency have a trade-off relation to each other, it is difficult for both of them to be individually and independently optimized.

On the other hand, a voltage variation range represents a voltage sensitivity and decides the dynamic range of the output terminal of the unit pixel. However, since the conventional unit pixel may not increase the voltage variation range, the dynamic range of the output terminal of the unit pixel is substantially limited.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide an image sensor that is characterized by an improved output dynamic range and respectable charge transfer and quantum efficiencies.

In accordance with an aspect of the present invention, there is provided an image sensor, comprising: a semiconductor substrate of a first conductivity type: a peripheral circuit formed on a first region of the semiconductor substrate, wherein a ground voltage level is applied to the first region; a unit pixel array having a plurality of unit pixels formed on a second region of the semiconductor substrate, wherein the first region is isolated from the second region and wherein a negative voltage level is applied to the second region;

and a negative voltage circuit configured to provide the negative voltage for the second region.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and aspects of the invention will become apparent from the following description of the embodiments with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram illustrating a unit pixel of a conventional CMOS image sensor;

Fig. 2 is a cross-sectional view illustrating a structure of the unit pixel in Fig. 1;

Fig. 3 is a circuit diagram illustrating a unit pixel of a CMOS image sensor according to the present invention;

Fig. 4 is a cross-sectional view illustrating a structure of the unit pixel in Fig. 3; and

Figs. 5A to 5D are cross-sectional views illustrating a method for fabricating the unit pixel in Fig. 4.

DETAILED DESCRIPTION OF THE INVENTION

Hereafter, the present invention will be described in detail with reference to the accompanying drawings.

As shown in Fig. 3, an image sensor of the present invention includes a peripheral circuit and a unit pixel. The peripheral circuit includes a negative voltage generator 302 and a load transistor 304. The peripheral circuit and the unit pixel are electrically isolated from each other. The semiconductor substrate of the peripheral circuit is set to a voltage level of ground and that of the unit pixel is configured to receive a negative voltage generated from the negative voltage generator 302 or via a negative voltage supplied from an external circuit through a pin of a chip.

It should be noted that the unit pixel of the present invention receives a negative voltage ($-V_{sub}$) from the negative voltage generator 302. A pinned photodiode (PDD) and a floating sensing node also receive the negative voltage, for example approximately -2V, from the negative voltage generator 302. Similarly, transfer, reset, drive and select transistors Tx, Rx, Dx and Sx receive the negative voltage. That is, the four transistors receive a reverse bias voltage.

The pinning voltage of the pinned photodiode may be set at a low level so that the charge transfer efficiency is increased. Also, although the pinning voltage of the pinned photodiode may be set at a low level, the semiconductor substrate has a negative voltage of -2V. Accordingly, if the pinning voltage of the pinned photodiode is set at a low level, the reverse bias voltage applied to the pinned photodiode is able to form a deep depletion layer.

The reset and transfer transistors Rx and Tx are made up of a native NMOS transistor so that the charge transfer efficiency is improved. A native NMOS transistor, which has about a zero threshold voltage, can prevent electron losses from being generated compared to an NMOS transistor having a positive threshold voltage. Hence, the use of native NMOS transistors helps to improve the charge transfer efficiency of the sensor. Since the reverse bias voltage is used in the unit pixel of the present invention, a threshold voltage of each transistor may be increased. Accordingly, when the transistors are designed, the threshold voltage should be considered. The threshold voltage of the transfer and reset transistors Tx and Rx should be decreased such that the photoelectric charges are efficiently transferred. N^+/P junction and MOS capacitor photodiodes, as an alternative to the pinned photodiode may be applied to the unit pixel of the present invention.

As shown in Fig. 4, it should be noted that an N-type buried layer is provided in a P-epi layer of the unit pixel, which is formed on a P^+ substrate (not shown), and the unit pixel is isolated from the P-epi layer of a peripheral circuit by the N-type buried layer. Also, it should be noted that a negative voltage is applied to the P-epi layer in which elements of the unit pixel are formed.

Various methods for applying a negative voltage to the P-epi layer may be used. For example, a P^+ diffusion region (not shown) made in a portion of the P-epi layer of the unit pixel, which is isolated from the P-epi layer of a peripheral circuit by the N-type buried layer, and a wire for applying a negative voltage to the P-epi layer is in contact with the P^+ diffusion region, so that a negative voltage may be applied to the P-epi layer of the unit pixel.

On the other hand, when unit pixels are isolated from each other by the N-type buried layer, each of the unit pixels needs the P^+ diffusing and wiring processes. The unit pixel array is divided by the N-type buried layer and a negative voltage is applied to the divided unit pixel array. At this time, field oxide layers are formed between the unit pixels and the unit pixels should be isolated from the peripheral circuit by the N-type buried layer. The P-epi layer of the unit pixel is surrounded by the N-type buried layer so that the P-epi

layer of the unit pixel is isolated from the P-epi layer of the peripheral circuit, and independently receives a negative voltage.

A pinned photodiode (PPD) and an N^+ floating junction FD are formed in the P-epi layer. The pinned photodiode senses light from an object and generates photoelectric charges. The N^+ floating junction receives the photoelectric charges from the pinned photodiode. To detect electrical signals from the N^+ floating junction FD, an output transistor having a positive threshold voltage is formed in a P-well of the P-epi layer. The output transistor is composed of drive and select transistors Dx and Sx. Also, in order to transfer the photoelectric charges from the pinned photodiode to the N^+ floating junction FD, the transfer transistor Tx having a negative threshold voltage is formed in the P-epi layer. The reset transistor Rx and a N^+ drain diffusion region DD, to which a power supply V_{DD} is applied, are formed in the P-epi layer. The N^+ floating junction FD and the N^+ drain diffusion region DD are composed of a heavily doped region in order to reduce an overlap capacitance with a gate electrode.

As shown in Figs. 5A to 5D, a method for fabricating a CMOS image sensor with the N-type buried layer is provided.

Referring to Fig. 5A, a P-epi layer 501 is formed on a P^+ substrate 500 and field oxide layers 502 are formed on the P-epi layer 501 between active regions by a LOCOS (local oxidation of silicon) process or a trench isolation process.

Referring to Fig. 5B, a mask pattern 503 is provided to expose what will comprise the active region of the unit pixel. After forming the mask pattern 503, a first N-type buried layer 505 is formed in the P-epi layer 501 using a P_{31}^+ (phosphor) ion implantation of N-type impurities at an acceleration energy of approximately 3 MeV.

Referring to Fig. 5C, a mask pattern 506 is formed between the field oxide layers 502. After forming the mask pattern 506, a second N-type buried layer 508a is formed beneath the field oxide layers 502. The P-epi layer 501 corresponding to the active region is surrounded by the first N-type buried layer 505 and the second N-type buried layer 508a. In addition, an N-well region 508 in a neighboring unit pixel may be formed at the time of forming the second N-type buried layer 508a.

Referring to Fig. 5D, after removing the mask patterns 503 and 506, a P-well mask pattern 509 is formed and a P-well region 511 is formed by a B_{11} (boron) ion implantation of P-type impurities.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications,

additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

WHAT IS CLAIMED IS:

1. An image sensor comprising:

a semiconductor substrate of a first conductivity type;

a peripheral circuit formed on a first region of the semiconductor substrate, wherein a ground voltage level is applied to the first region;

a unit pixel array having a plurality of unit pixels formed on a second region of the semiconductor substrate, wherein the first region is isolated from the second region and wherein a negative voltage level is applied to the second region; and

a negative voltage circuit configured to provide the negative voltage for the second region.

2. The image sensor as recited in claim 1, wherein the image sensor comprises a buried layer isolating each of the unit pixels so that the buried layer surrounds the unit pixels.

3. The image sensor as recited in claim 2, wherein the semiconductor substrate comprises a P^+-type substrate and a P-type epitaxial layer which is formed on the P^+-type substrate, wherein the buried layer is formed in the P-type epitaxial layer.

4. The image sensor as recited in claim 3, wherein the negative voltage circuit comprises a P^+ diffusion layer which is formed in the P-type epitaxial layer and wherein the negative voltage is applied to the P^+ diffusion layer.

5. The image sensor as recited in claim 4, wherein the P^+ diffusion layer is shared with the second region of neighboring pixels.

6. An image sensor, comprising:

a plurality of unit pixels formed in a first region of a substrate that is biased at a ground reference, each pixel surrounded by a first epitaxial layer that is biased at a negative potential relative to the ground reference; and

a bias generator formed in a second region of the substrate that is biased to the ground reference.

7. An image sensor, comprising:

a substrate having a first conductivity type;

a plurality of unit pixels formed in a first region of the substrate; and

a peripheral circuit formed in a second region of the substrate, the peripheral circuit operable to generate a negative voltage relative to a ground reference, wherein the first region is biased at the negative voltage and the second region is biased at the ground reference.

8. The image sensor of claim 7, wherein the first and second regions have a second conductivity type.

9. The image sensor of claim 7, wherein each unit pixel comprises a photodiode that is reverse biased at the negative voltage.

10. The image sensor of claim 9, wherein each unit pixel further comprises:

a transfer transistor having a gate controlled by a transfer signal, a source coupled to the photodiode, a body biased at the negative voltage and a drain coupled to a sense node.

11. The image sensor of claim 10, wherein each unit pixel further comprises a capacitor having a first end coupled to the sense node and a second end coupled to the negative voltage.

12. The image sensor of claim 11, wherein each unit pixel further comprises a reset transistor having a gate controlled by a reset signal, a source coupled to the sense node, a drain coupled to a positive power supply and a body biased at the negative voltage.

13. The image sensor of claim 12, wherein each unit pixel further comprises a drive transistor having a gate coupled to the sense node, a drain coupled to the positive power supply, a body biased at the negative voltage and a source.

14. The image sensor of claim 13, wherein each unit pixel further comprises a select transistor having a gate controlled by a select transistor, a drain coupled to the source of the drive transistor, a body biased at the negative voltage and a source embodying an output of the unit pixel.

15. A method of improving the charge transfer efficiency of a photodiode device, the method comprising the steps of:

providing a ground reference;

providing a bias generator for generating a negative potential relative to the ground reference; and

providing a photodiode device having a photodiode including a p-type side that is electrically coupled to the negative potential.

IMAGE SENSOR WITH IMPROVED DYNAMIC RANGE BY APPLYING NEGATIVE VOLTAGE TO UNIT PIXEL

ABSTRACT OF THE DISCLOSURE

The present invention is to provide an image sensor, including: a semiconductor substrate of a first conductive type: a peripheral circuit formed on a first region of the semiconductor substrate, wherein a ground voltage level is applied to the first region; a unit pixel array having a plurality of unit pixels formed on a second region of the semiconductor substrate, wherein the first region is isolated from the second region and wherein a negative voltage level is applied to the second region; and a negative voltage generator for providing the negative voltage for the second region.

FIG. 1
(PRIOR ART)

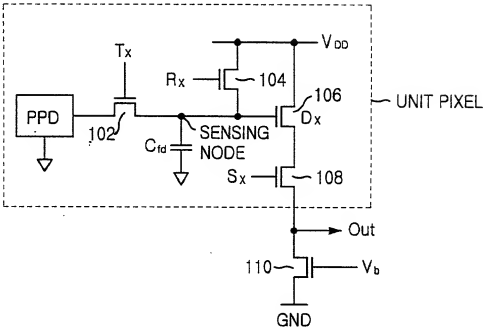


FIG. 2
(PRIOR ART)

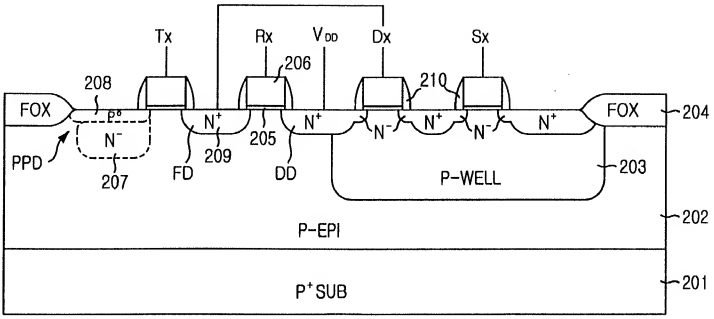
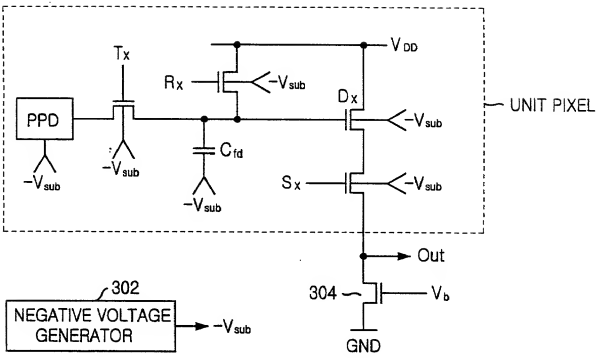


FIG. 3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PPD
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NEGATIVE VOLTAGE GENERATOR
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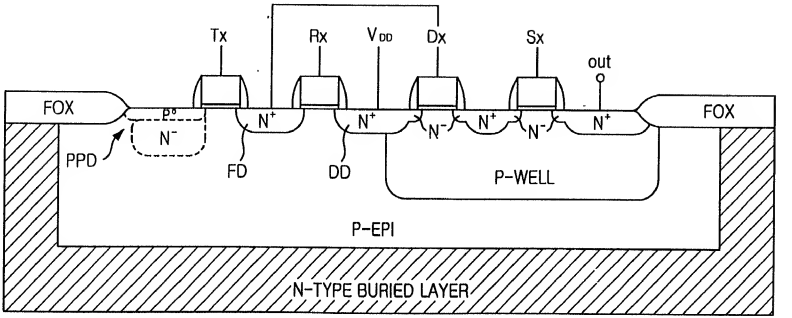
FIG. 4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N^-
N^+
P-WELL
P-EPI
N-TYPE BURIED LAYER

FIG. 5A

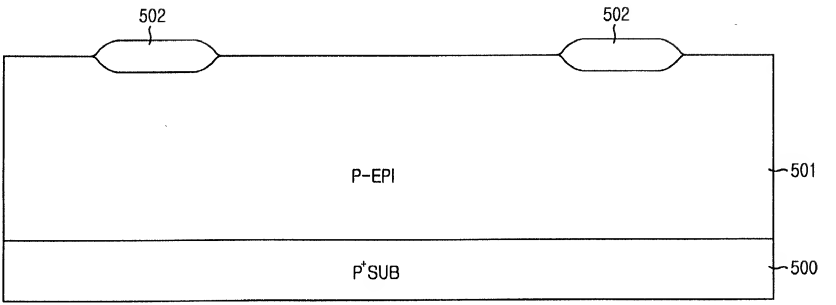

FIG. 5B

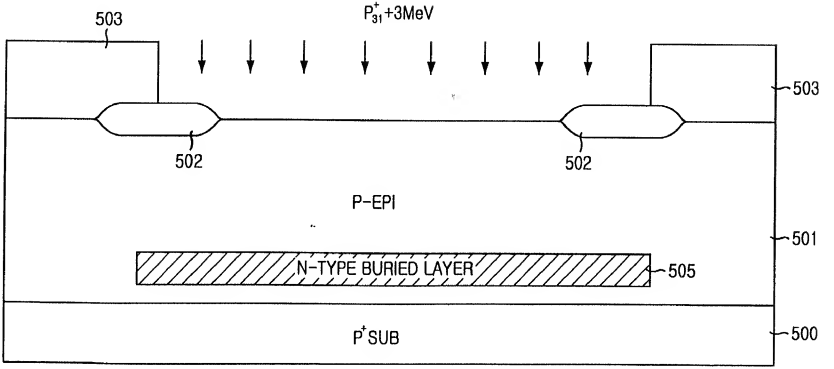
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FIG. 5C

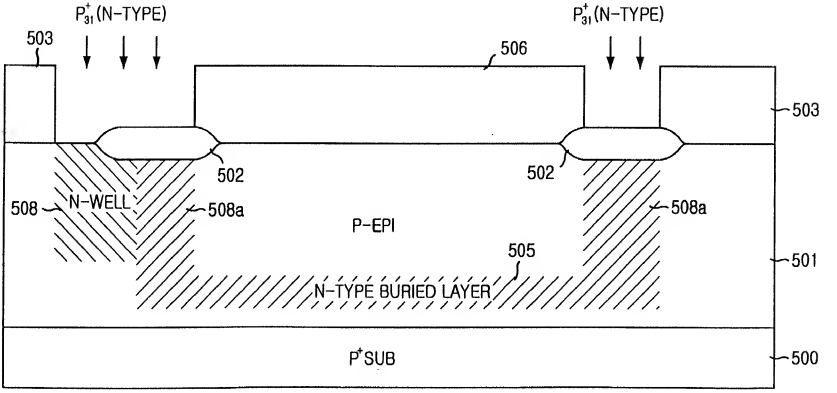
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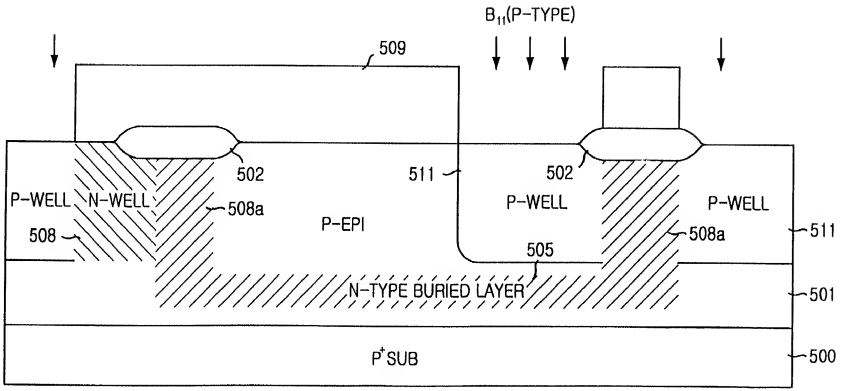
FIG. 5D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511
505
N-TYPE BURIED LAYER
501
P^+SUB
500

Attorney Docket No.: 0939H-071110US
Client Reference No.: P99H4027/US/JJ

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **IMAGE SENSOR WITH IMPROVED DYNAMIC RANGE BY APPLYING NEGATIVE VOLTAGE TO UNIT PIXEL** the specification of which __X__ is attached hereto or ____ was filed on _____ as Application No. _____ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

P · oreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I ·y claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

· the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the ·t matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by ·st paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in ·7, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or ·nternational filing date of this application:

Application No.	Date of Filing	Status
09/343,096	June 29, 1999	Pending

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

ture of Inventor 1	Signature of Inventor 2
ol Chung	Seong Dong Kim
	Date

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